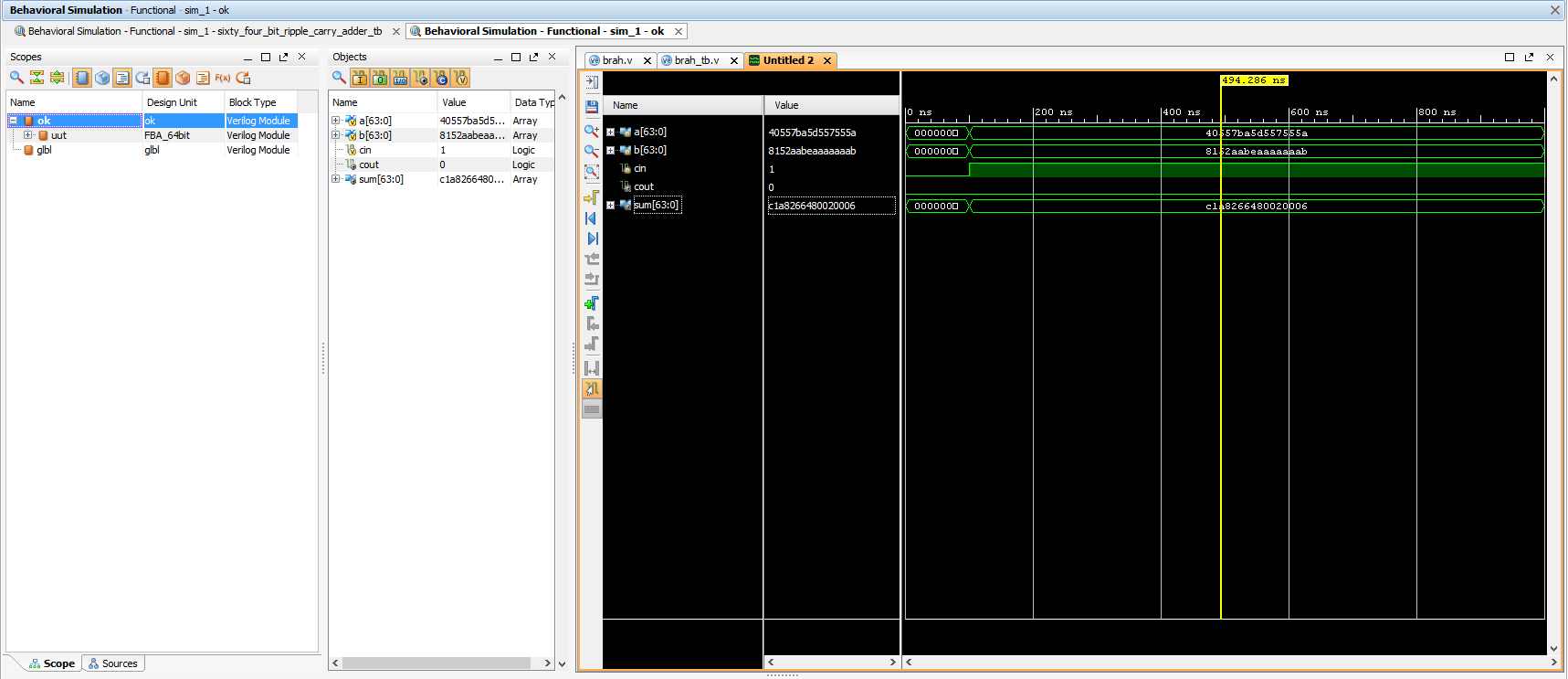
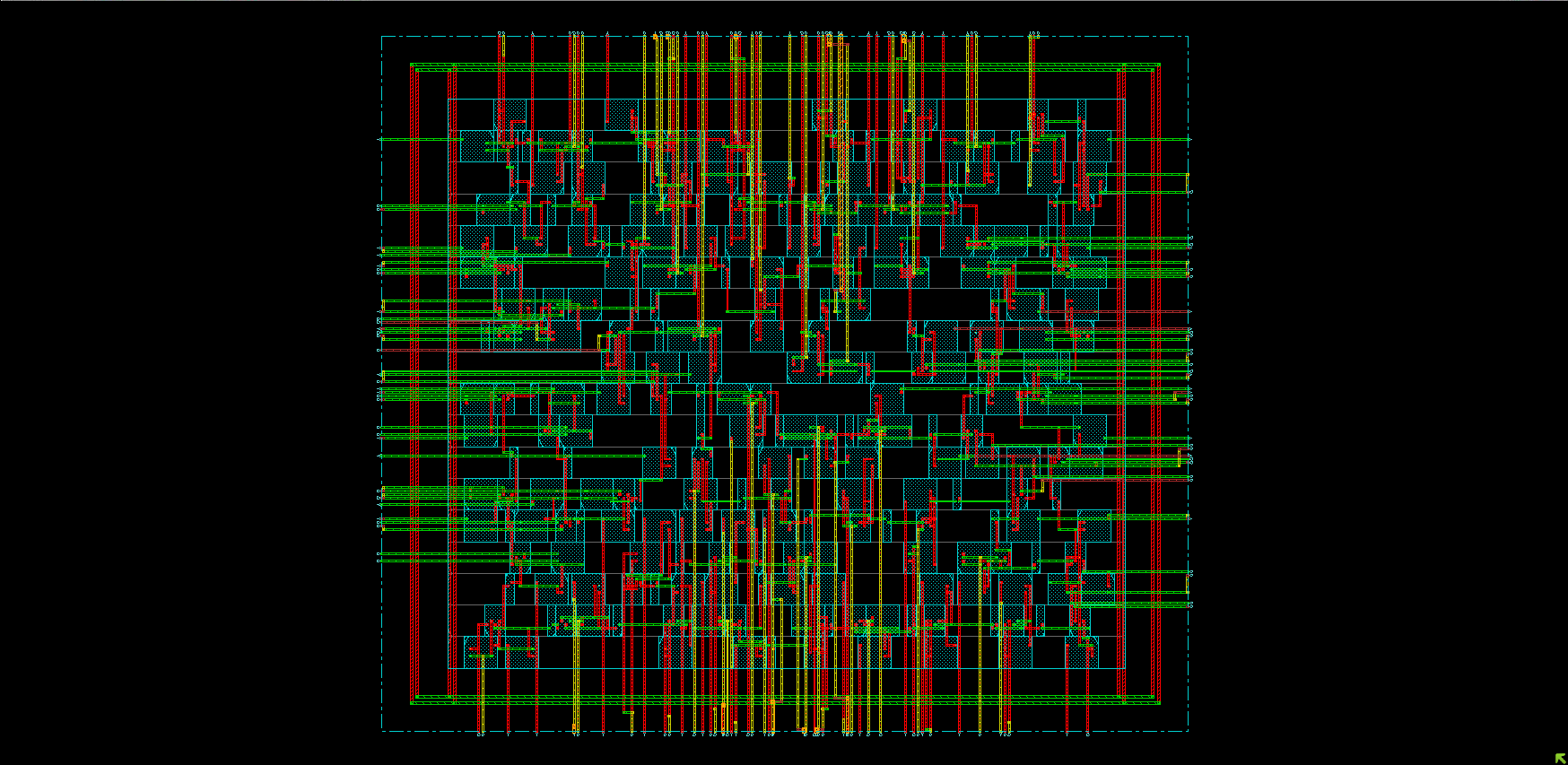
Jomar Pueyo UXT302

Location: /home/UTSARR/uxt302/Lab7\_64bitadder/

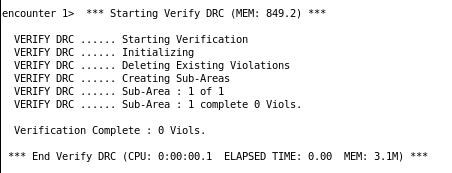
LAB 7: 64-Bit Ripple Adder

Waveform: 

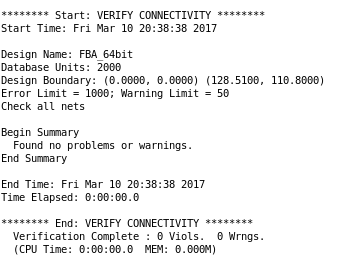
Chip Layout:



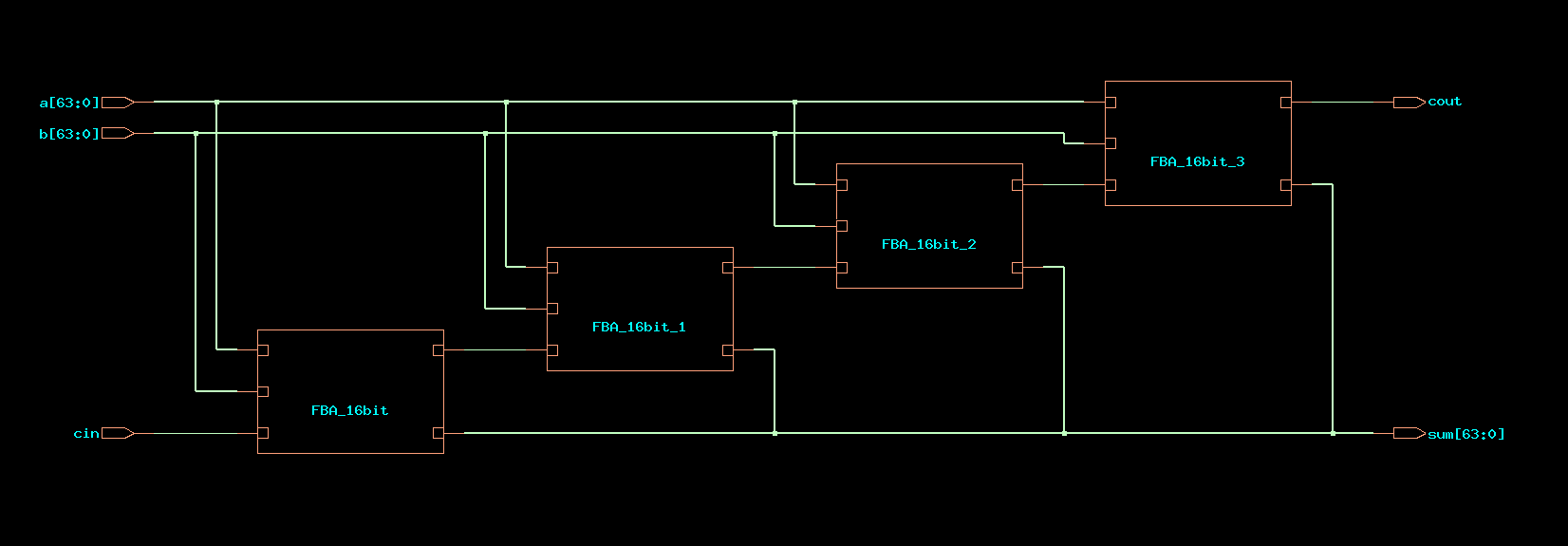
Verify DRC:



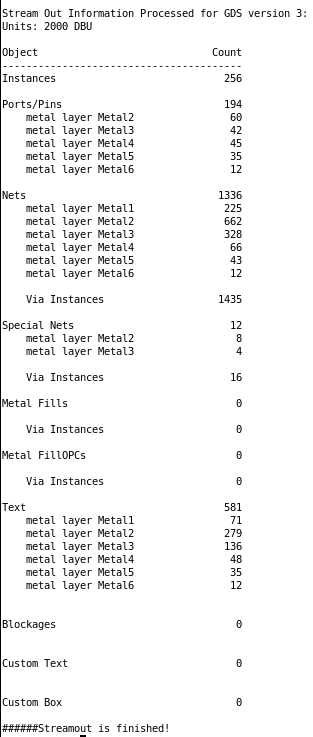
Verify Connectivity:



Schematic:



GDS “Streamout is successful”:



**Table:**

|  |  |
| --- | --- |
| **Area** | |
| Total cells used in design | 250 |
| Cell area | 4817 |
| **Pre-Route** | |
| CPU Time | 0.25 sec |
| Memory Usage | 800.195 Mbytes |
| **Post-Route** | |
| CPU Time | 0.28 sec |
| Memory Usage | 806.473 Mbytes |

F:\VLSI\Lab Assignment 7\Cell Area.PNG

F:\VLSI\Lab Assignment 7\Pre-Timing.PNG

F:\VLSI\Lab Assignment 7\Post-Timing.PNG